



SE-7403

**B. E. IV (Sem. VII) (Elect.) Examination**  
**April / May – 2011**  
**Microprocessor & Its Applications to**  
**Electrical Engg.**

Time : 3 Hours]

[Total Marks : 100

**Instructions :**

(1)

नीचे दर्शायेव निशानीवाणी विगतो उत्तरवही पर अवश्य कपवी. Fillup strictly the details of signs on your answer book.	Seat No. :
Name of the Examination :	<input type="text"/>
<input type="checkbox"/> B. E. 4 (Sem. 7) (Elect.)	<input type="text"/>
Name of the Subject :	<input type="text"/>
<input type="checkbox"/> Microprocessor & Its Applications to Electrical Engg.	<input type="text"/>
Subject Code No. : <input type="text"/> 7 <input type="text"/> 4 <input type="text"/> 0 <input type="text"/> 3	<input type="text"/>
Section No. (1, 2,.....): <input type="text"/> 1&2	<input type="text"/>
	Student's Signature

- (2) Attempt all questions.
- (3) Answers to the two sections must be written in separate answer books.
- (4) Figures to the right indicate full marks.
- (5) Assume any data if needed.

**SECTION - I**

- 1 (a) Fill in the blanks : 6
- (1) \_\_\_\_\_ address lines are required to address 16 k Memory.
  - (2) ALE signal is used to be multiplex \_\_\_\_\_ address lines.
  - (3) 8085 can access maximum \_\_\_\_\_ memory locations because it has \_\_\_\_\_ address lines.
  - (4) RST 4 has \_\_\_\_\_ internal memory address.
  - (5) MSE stands for \_\_\_\_\_.
  - (6) \_\_\_\_\_ is a Programmable Communication Interface.
- (b) Define T-state and instruction cycle. 4
- (c) Why Buffer is required in interfacing ? 3

- (d) Explain following pins of 8085 : 4
- (i) ALE
- (ii) Ready
- (e) Draw and explain memory; write machine cycle. 3
- 2 Attempt any two : 15**
- (1) Design an interfacing scheme having two 8 k EPROM and eight 8 k RAM using suitable decoder. Also show its memory map.
- (2) Draw Timing diagram for LDA 8000 h and show all necessary signals.
- (3) Explain 8279 with the help of block diagram.
- (4) Draw an interfacing scheme to interface one common anode seven segment display and write a program to display '0' on it.
- 3 Attempt any three : 15**
- (1) Draw and explain timing diagram of OUT 10 h instruction.
- (2) Explain all steps that take place when an interrupt comes. List also all available interrupts in 8085.
- (3) Explain mode 1 operation of 8255.
- (4) Draw and explain each block of 8254.
- (5) Draw and explain interfacing scheme to interface 8255 with 8085.

## SECTION - II

- 4 (a) Fill in the following blanks :**
- (1) TRAP interrupt has vector address \_\_\_\_\_. 1
- (2) OUT 25 h is \_\_\_\_\_ byte instruction. 1
- (3) The addressing mode of LDAX B is \_\_\_\_\_. 1
- (4) JNC 3000 H instruction checks the status of \_\_\_\_\_ flag to divert the flow of program sequence. 1



- 5 (a) Write a program to perform following multibyte decimal 8  
addition  $45678932 + 56789887$
- (b) A set of certain data byte is stored in memory starting 7  
from C100H. The data string is terminated by FFH.  
Write a program that checks each data byte for positive  
or negative rejects negative data adds all positive data  
and store the 16-bit result in memory starting from  
C130H.
- 6 (a) Draw an interfacing scheme to interface ADC0804 with 9  
8085 and hence write a program to read 100 samples  
from ADC with 50 ms time interval.
- (b) Write a program to find out the lowest and highest 6  
number from the given set of data. Store both the  
numbers in consecutive memory locations.

**OR**

- 6 (a) What are different software and hardware interrupts 9  
associated with 8085 ? Explain internal block diagram  
of 8085 interrupt system alongwith the priority of  
various interrupts and the memory map of their vector  
location.
- (b) Draw and explain block diagram of 82534. Explain its 6  
control word format. List various modes in which 8253  
can operate and explain its interfacing with 8085.